

Graphics Digitizer

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ABSTRACT

A graphics digitizer having a phase-locked-loop, a timing generator, and at least one channel with a reference and bias voltage generator and an analog-to-digital converter is disclosed. In some embodiments, the phase-locked-loop includes a programmable Div/N circuit so that the output frequency of the signal generated by the phase-locked-loop is programmable. In some embodiments, the timing generator generates a HSOUT video signal in response to the HSYNC video signal by sampling the HSYNC video signal with a phase adaptively chosen in response to a programmable phase between the signal generated by the phase-locked-loop and the HSYNC video signal. In some embodiments of the invention the reference and bias voltage generates a reference voltage determined by a digital-to-analog conversion of a value stored in a programmable gain register and generates a bias voltage proportionally to the reference voltage by a current digital-to-analog conversion of a value stored in a programmable offset register. In some embodiments of the invention, the analog-to-digital converter includes a pre-amp bank which is offset canceled at the end of each line of video signal. In some embodiments of the invention, the analog-to-digital converter includes a pre-amp bank where individual pre-amps are offset canceled randomly with each clock cycle. In some embodiments of the invention, the analog-to-digital converter includes a folding and interpolating circuit having a first folder and a second folder with the first folder utilizing voltage averaging as well as resistive interpolation in order to reduce offsets while the second folder utilizes resistive interpolation. In some embodiments of the invention, the analog-to-digital converter includes a comparator bank where each comparator is followed by an RS latch. In some embodiments of the invention, the analog-to-digital converter includes a digital encoder where the most significant bits are determined by counting the number of a set of course comparator outputs which are at a first level and the

least significant bit are determined by counting the number of a set of fine comparator
outputs which are at a first level or at a second level, depending on the region of the range of
the analog-to-digital converter. In some embodiments of the invention, the analog-to-digital
converter includes a digital encoder having error correction. In some embodiments of the
5 invention, the analog-to-digital converter includes a digital encoder having range correction.

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